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(54) Bit erasable electrically erasable programmable read only memory.

(57) A bit erasable EEPROM is constructed which alleviates the problems of early termination of erasure and over-erasure. Rather than erasing the entire array at once, and thereby causing the problem of early termination of erasure and over-erasure, each cell is erased individually. In another embodiment of this invention, a group of one or more cells on a word line are erased at once with self-termination of the erase operation of each cell occurring when that cell's transistor becomes conductive, and at that time the erasure of only that cell ceases. The erasure of a particular cell ceases without effecting the erasure of operation of other cells. Therefore, the electrical erasure is self-limiting for each individual cell. In another embodiment of this invention, a group of one or more cells on a bit line are erased at once with no danger of under or over-erasure of each particular cell.

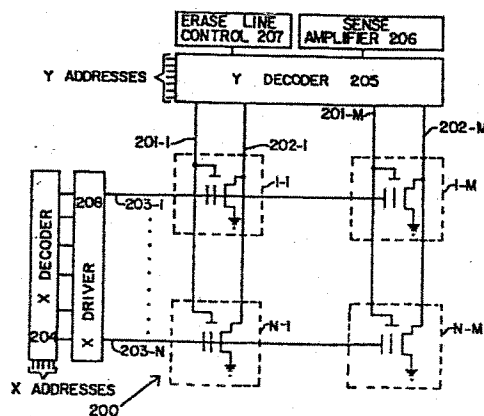


FIG. 4

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BIT ERASABLE ELECTRICALLY  
ERASABLE PROGRAMMABLE READ ONLY MEMORY

Andrew C. Tickle

BACKGROUND OF THE INVENTION

Field of the Invention

This invention relates to semiconductor memory devices and more particularly to programmable read only memory devices which are capable of being electrically erased.

Description of the Prior Art

Semiconductor memory devices are well known in the prior art. Programmable read only memories (PROMS) comprise a plurality of cells, each cell capable of storing a single binary digit (bit). The programmable read only memory (PROM) devices are capable of being programmed (i.e. each cell set to store either a logical 1 or a logical 0) after the device has been fabricated. It is often desirable to reprogram memory devices in order to alter the data stored within the memory device. Accordingly, erasable PROM devices have been developed. One such erasable programmable read only memory (EPROM) device is erased by exposing the device to ultraviolet light for several hours to discharge (i.e. erase) the memory cells. Another type of memory device is the electrically erasable programmable read only memory (EEPROM). The use of EEPROMS is highly desirable in that inexpensive packaging may be used because the memory device need not be capable of being exposed to ultraviolet light. Furthermore, EEPROMS are more easily erased than ultraviolet erasable EPROMS, because EEPROMS are capable of being erased in a matter of seconds. One such EEPROM is disclosed in European Patent Application 81401794.3 published on 26 May 1982 with publication number 0052566 and assigned to Fairchild Camera and Instrument Corporation.

1 Another such EEPROM device is described by Kupec et  
2 al in an article entitled "Triple Level Poly Silicon  
3 E<sup>2</sup>PROM with Single Transistor Per Bit", published in the  
4 Technical Digest of the International Electronic Devices  
5 Meeting, 1980, Washington, D.C., pages 602-606. The Kupec  
6 et al. cell structure is shown in Figures 1a-1d. As seen  
7 in Figure 1a, cell 100, is formed in a P-type substrate 1  
8 and includes N type diffused regions 2 and 3 which form  
9 the source-drain regions of the floating gate transistor 99  
10 of cell 100. Contact regions 9 and 8 allow electrical  
11 connection from low resistivity interconnect lines (not  
12 shown) to source-drain regions 2 and 3, respectively.  
13 Floating gate 5 is separated from substrate 1 by dielec-  
14 tric 10 and overlies the P type channel region 16 formed  
15 between N type source-drain regions 2 and 3. Formed above  
16 floating gate 5 is conductive word line 7 which also  
17 serves as the control gate of the transistor 99. Word  
18 line 7 is separated from floating gate 5 by dielectric 6.  
19 Erase line 11 is formed above and surrounding both floating  
20 gate 5 and word line 7. Each of the conductive layers 5,  
21 7 and 11 are separated from the others and the substrate  
22 by insulation layers 10, 6 and 12. As will be more fully  
23 described later, floating gate 5 stores a charge, thereby  
24 establishing the control gate threshold voltage of tran-  
25 sistor 99 and storing the desired data within memory  
26 cell 100.

27  
28 Figure 1b is a cross-sectional view taken along line  
29 BB shown in Figure 1a. As shown in Figure 1b, a layer of  
30 field oxide 10 is formed on P type silicon substrate 1.  
31 Floating gate is formed on field oxide 10 and covered by  
32 insulating layer 6 (typically oxide). Word line 7 is  
33 formed above and apart from floating gate 5. Floating  
34 gate 5, oxide 6, and word line 7 are surrounded by dielec-  
35 tric layer 12 (again typically oxide). Erase line 11 is  
36 formed above and around oxide 12 as shown.

37  
38

1        Figure 1c shows a cross-sectional view of the structure  
2 of Figure 1a taken along line CC. As shown in Figure 1c,  
3 field oxide 10 is formed on a P-type substrate 1 thereby  
4 defining the active area of the device having N-type  
5 source-drain regions 2 and 3. Gate oxide 4 is formed  
6 above the channel region located between source-drain  
7 regions 2 and 3. Floating gate 5 is formed above gate  
8 oxide 4 and covered by oxide 6, upon which word line 7 is  
9 formed. Word line 7 serves as the gate of transistor 99.  
10 Oxide 12, which serves as electrical insulation, is formed  
11 above and surrounding gate oxide 4, floating gate 5,  
12 oxide 6, and word line 7. Contact openings 8 and 9 are  
13 formed in order to allow electrical connection between low  
14 resistivity electrical leads (not shown) and source-drain  
15 regions 3 and 2, respectively.  
16

17        Figure 1d shows the symbolic representation of the  
18 floating gate memory cell 100 of Figure 1a. As shown in  
19 Figure 1d, floating gate memory cell 100 includes source-  
20 drain regions 2 and 3, floating gate 5, control gate 7 and  
21 erase line 11.  
22

23        Programming of cell 100 is accomplished by estab-  
24 lishing a charge on floating gate 5, which determines the  
25 threshold voltage of transistor 99. For example, a  
26 logical 1 is defined as a low impedance between source-  
27 drain regions 2 and 3 when a voltage of approximately 5  
28 volts is applied to control gate 7. Conversely, a  
29 logical 0 is defined as a high impedance between source-  
30 drain regions 2 and 3 when a voltage of approximately 5  
31 volts is applied to control gate 7. Accordingly, to  
32 program a logical 0 state in cell 100, electrons are  
33 stored on floating gate 5 by conventional channel injec-  
34 tion of hot electrons. This is accomplished, for example,  
35 by placing a high voltage (typically 10 to 20 volts) on  
36 control gate 7, placing a relatively high voltage (typically  
37 10 to 20 volts) on source-drain region 3, and grounding  
38

1 source-drain region 2 and erase line 11. This causes  
2 electrons to flow to source-drain region 3 from source-  
3 drain region 2 and, in the process, some electrons are  
4 injected from the channel region 16 through gate oxide 4  
5 to floating gate 5. During this programming of cell 100  
6 to a logical zero, sufficient electrons are stored within  
7 floating gate 5 to bias memory cell 100 such that a 5 volt  
8 signal applied to control gate 7 will be insufficient to  
9 cause transistor 99 to turn on. Conversely, a logical 1  
10 state is provided by the absence of electrons stored on  
11 floating gate 5, thus allowing a 5 volt signal placed on  
12 control gate 7 to cause transistor 99 to turn on.  
13

14 Erasing memory cell 100 is accomplished by removing  
15 the electrons within floating gate 5, thereby returning  
16 floating gate 5 to ground potential. This erasure is  
17 accomplished, for example, by grounding source-drain  
18 region 3 and control gate 7. A high voltage (typically 10  
19 to 20 volts) is placed on the erase line 11, thus causing  
20 electrons stored within floating gate 5 to tunnel through  
21 regions 15 of oxide 12 to erase line 11.  
22

23 Figure 2 shows a typical array 300 of NxM memory  
24 cells 1-1 through N-M, where N is the number of words in  
25 the array and M is the number of bits per word. Accord-  
26 ingly, memory array 300 is shown having cell 1-1, providing  
27 the first bit of word 1, memory cell 1-M, providing the  
28 Mth bit of word 1, cell N-1, providing the first bit of  
29 the Nth word, and cell N-M, providing the Mth bit of the  
30 Nth word. Each of the cells 1-1 through N-M of memory  
31 array 300 comprise, for example, EEPROM cells identical to  
32 cell 100 shown in Figure 1a. Memory array 300 includes X-  
33 decoder 304, X driver 308, Y decoder 305, and sense  
34 amplifier 306. X decoder 304 serves to receive a binary  
35 input word defining which word line 303-1 through 303-N is  
36 to be selected. X decoder 304 allows an X word comprising  
37 n bits to define which of the  $N=2^n$  word lines 303-1 through  
38

1 303-N is to be selected. X driver 308 serves to provide  
2 the appropriate voltages on the selected word lines  
3 303-1 through 303-N, and on the remaining deselected word  
4 lines. Y decoder 305 serves the same function in decoding  
5 an m bit input word defining which of the  $M=2^m$  pairs of  
6 bit lines 301-1, 302-1 through 301-M, 302-M is to be selected.  
7 Sense amplifier 306 serves, during the read operation, to  
8 determine the state of the cell being read. Naturally, as is  
9 well known to those of ordinary skill in the art, memory array 300  
10 may include a plurality of sense amplifiers 306 thus  
11 allowing a plurality of cells along a selected word line  
12 to be read or written simultaneously, although such  
13 additional sense amplifiers are not shown in the figures  
14 for the sake of brevity.

15  
16 To program the cells on a selected word line, for  
17 example word line 303-1, a high voltage is placed on the  
18 selected word line 303-1. This places a high voltage  
19 (typically 10-20 volts) on each control gate 7 of each  
20 cell 1-1 through 1-M. Those cells 1-1 through 1-M that  
21 are to be programmed to store a logical 0 have a high  
22 voltage placed on their associate bit lines 302-1 through  
23 302-M by Y decoder 305 and those cells 1-1 through 1-M  
24 which are to be programmed to store a logical 1 have their  
25 bit lines placed at ground. The Y decoder 305 receives a  
26 signal from external circuitry (not shown) which determines  
27 which cells are to be programmed to store a logical 0 and  
28 which cells are to be programmed to store a logical 1 and  
29 selectively applies the proper potential to the bit lines  
30 302-1 through 302-M for proper programming. Likewise, the  
31 X decoder 304 receives a similar signal, determines which  
32 word line is to have its cells programmed and, through the  
33 X driver 308, applies the appropriate voltage to the  
34 selected word line and to the remaining deselected word  
35 lines to the proper word line 303.

36  
37  
38

1        To read the data stored within the cells of a desired  
2 word line of array 300, for instance, word line 303-1, a  
3 potential is applied to word line 303-1. This potential  
4 is typically 2-5 volts which is sufficient to cause each  
5 cell storing a logical 1 (and which have a lower control  
6 gate threshold voltage) to turn on, but is insufficient to  
7 cause each cell storing a logical 0 (and which have a  
8 higher control gate threshold voltage to turn off). A  
9 potential is applied to each of the bit lines 302-1 to  
10 302-M. Those cells 1-1 through 1-M which have been pro-  
11 grammed to store a logical 1 will then be conductive,  
12 while those that are programmed to store a logical 0 will  
13 not. The sense amplifier 306 determines which cells are  
14 conductive (and therefore have grounded bit lines) and  
15 which are not and supplies this data to external circuitry  
16 (not shown). The other word lines 303-2 to 303-N are kept  
17 at ground potential, and therefore the cells along those  
18 word lines do not become conductive, regardless of the  
19 data stored in each cell and their control gate threshold  
20 voltage.

21  
22        One particular problem experienced with such prior  
23 art techniques for erasing arrays of memory cells, wherein  
24 each cell in the array is erased simultaneously, is that  
25 electrical erasure of each cell is not self-limiting. In  
26 other words, in an array of a plurality of memory cells,  
27 each memory cell will not behave in an identical manner  
28 during erase. Thus, while one cell within such a memory  
29 array may be erased with a voltage of 15 volts applied to  
30 its erase line, another memory cell may not be erased with  
31 this low a voltage, and yet another memory cell may be  
32 over-erased in that sufficient electrons are withdrawn  
33 from its floating gate to place its floating gate at a  
34 positive potential rather than at ground, as desired.  
35 Thus, electrical erasure of an array of memory cells can  
36 result in the storage of undesired data within the memory  
37 array.

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1        One attempt to overcome this problem created by the  
2 non-uniform nature of electrical erasure of a plurality of  
3 EEPROM cells has been discussed in the above-mentioned  
4 article of Kupec et al. An EEPROM device comprising an  
5 array of EEPROM cells constructed in accordance with the  
6 Kupec et al. article is shown in the schematic diagram of  
7 Figure 3. Figure 3 shows an array of  $N \times M$  memory cells,  
8 wherein  $N$  is the number of words in the array, and  $M$  is  
9 the number of bits per word. During erasure of the Kupec  
10 et al. structure of Figure 3, the erase lines 11-1 through  
11 11- $M$  are connected in common with each of the bit lines  
12 13-1 through 13- $M$  which are in turn connected through  
13 resistor 14 to terminal 19 which is connected to the erase  
14 voltage  $VE$ . During erasure, the erase voltage  $VE$   
15 (typically 10 to 20 volts) is applied through resistor 14  
16 to erase lines 11 and bit lines 13. Each word line 7-1  
17 through 7- $N$  is held low (typically ground). The drain of  
18 each memory cell 1-1 through  $N-M$  is connected to bit line  
19 13 and the source of each memory cell 1-1 through  $N-M$  is  
20 connected to ground. Thus, during erasure, the high  
21 voltage applied to erase lines 11-1 through 11- $M$  causes  
22 electrons to tunnel from the floating gates of the cells  
23 1-1 through  $N-M$  to erase lines 11-1 through 11- $M$  respec-  
24 tively, thus tending to discharge the floating gates of  
25 each memory cell 1-1 through  $N-M$  of array 101. However,  
26 when a single one of memory cells 1-1 through  $N-M$  is  
27 sufficiently erased such that that cell begins to conduct  
28 (i.e. current flows from its source connected to its  
29 associated bit line through its channel to its source  
30 terminal connected to a voltage below the effective erase  
31 voltage, thereby ceasing erasure), bit lines 13-1 through  
32 13- $M$  are reduced in potential. Because bit lines 13-1  
33 through 13- $M$  and erase lines 11-1 through 11- $M$  are connected  
34 in common during erase, erase lines 11-1 through 11- $M$  are  
35 also reduced in potential when a single cell 1-1 through  
36  $N-M$  is sufficiently erased to turn on. At this time,  
37 erasure of all memory cells 1-1 through  $N-M$  of memory  
38



1 array 101 ceases, regardless of whether each memory cell  
2 1-1 through N-M is in fact sufficiently erased. Thus,  
3 while this erasure technique prevents the over erasure of  
4 cells 1-1 through N-M, this erasure technique results in  
5 the nonsymmetrical erasure of memory cells 1-1 through N-M,  
6 with the resultant aforesaid problem of undesirable data  
7 remaining stored within certain memory cells of memory  
8 array 101.

9  
10 Compounding the problem of nonsymmetrical erase charac-  
11 teristics of manufactured devices, the voltage required  
12 for erasure typically increases, often by more than a  
13 factor of 2, after repeated (approximately 10,000) write  
14 and erase cycles. Since in most operating conditions some  
15 cells of the memory array will never (or seldom) be written  
16 into, these cells will not experience any degradation in  
17 erase conditions due to tunneling currents during erasure,  
18 and therefore, these cells will, over a long period of  
19 time, retain their ability to be erased at a relatively  
20 low erase voltage. Thus, these cells will terminate the  
21 erase operation before the more heavily exercised cells,  
22 which have been repeatedly written and erased and thus  
23 have degraded erase characteristics requiring higher erase  
24 voltages, are fully erased.

25  
26 SUMMARY

27  
28 In accordance with this invention, a bit erasable  
29 EEPROM is constructed which alleviates the problems of  
30 early termination of erasure and over-erasure. Rather  
31 than erasing the entire array at once, and thereby causing  
32 the problem of early termination of erasure and over-erasure  
33 mentioned above, according to one embodiment of the present  
34 invention each cell is erased individually. In another  
35 embodiment of this invention, a group of one or more cells  
36 on a word line are erased at once with no danger of under  
37 or over-erasure of each particular cell. Self-termination  
38

1 of the erase operation of each cell occurs when that  
2 cell's transistor becomes conductive, and at that time the  
3 erasure of only that cell ceases. The erasure of a parti-  
4 cular cell ceases without effecting the erasure of operation  
5 of other cells. Therefore, the electrical erasure is  
6 self-limiting for each individual cell.  
7

8 In accordance with another embodiment of this invention,  
9 a group of one or more cells on a bit line are erased at  
10 once with no danger of under or over-erasure of each  
11 particular cell.  
12

#### 13 BRIEF DESCRIPTION OF THE DRAWING

14  
15 Figure 1a is a plane view of a typical EEPROM cell;  
16

17 Figure 1b is a cross-sectional view taken long the  
18 line BB of Figure 1a.  
19

20 Figure 1c is a cross-sectional view of the structure  
21 of Figure 1a taken along the line CC;  
22

23 Figure 1d shows the symbolic representation of the  
24 floating gate memory cell 100 of Figure 1a;  
25

26 Figure 2 is a schematic diagram of a typical prior  
27 art EEPROM array;  
28

29 Figure 3 is a schematic diagram of a prior art EEPROM  
30 array during erase; and  
31

32 Figure 4 is a schematic diagram of one EEPROM array  
33 constructed in accordance with this invention.  
34

#### 35 DETAILED DESCRIPTION

36  
37 Prior art EEPROM devices, as discussed above, terminate

1 erasure when current begins to flow in the erase or bit  
2 line of the memory array due to the erasure of a single  
3 cell, possibly resulting in incomplete erasure of the  
4 remaining cells of the array. In contrast, the present  
5 invention alleviates this problem of insufficient or  
6 over-erasure by allowing each cell along an individual bit  
7 line to be independently erased. However, each cell along  
8 a particular word line is erased along with the other  
9 cells along that particular word line without the danger  
10 of over or insufficient erasure.

11  
12 Figure 4 shows one embodiment of an EEPROM construc-  
13 ted in accordance with the principles of this invention..  
14 Memory array 200, of size  $N \times M$ , includes erase lines 201,  
15 bit lines 202-1 through 202-M word lines 203-1 through  
16 203-N, X decoder 204, Y decoder 205, sense amplifier 206,  
17 erase line control 207, X driver 208 and cells 1-1 through  
18 N-M. As in the circuit of Figure 2, N is the number of  
19 words in the array and M is the number of bits per word.  
20 In this embodiment of the invention, each individual cell  
21 is selectively erased without effecting the programmed  
22 state of any other cell. This is a significant improve-  
23 ment over prior art EEPROM arrays which required the  
24 simultaneous erasure of all cells along an entire word  
25 line.

26  
27 In order to erase a desired cell, for example cell  
28 1-1, the erase voltage pulse VE (typically 10-20 volts) is  
29 applied for a short period of time (i.e., typically 1  
30 millisecond) through the Y decoder to the selected erase  
31 line 201-1 and to the selected bit line 202-1. The word  
32 line 203-1 corresponding to the cell 1-1 to be erased is  
33 held at a low voltage, typically ground. The remaining  
34 word lines 203-2 through 203-N do not contain cells which  
35 are to be erased and are held at a high voltage (typically  
36 10-20 volts). This high voltage is capacitively coupled  
37 to the floating gates of the cells which are not to be  
38

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1 erased, thereby reducing the voltage difference between  
2 the erase electrode and the floating gate of each cell  
3 which is not to be erased to a value below the voltage  
4 difference required to cause tunnelling between the float-  
5 ing gate and the erase terminal. Thus, all cells on  
6 deselected word lines 203-2 through 203-N are not erased.

7  
8 A portion of the electrons held on the floating gate  
9 of cell 1-1 are injected from the floating gate to the  
10 erase line 201-1 of cell 1-1 in response to each erase  
11 voltage pulse. As this is done, cell 1-1 will, after a  
12 sufficient number of erase pulses, have its control gate  
13 threshold voltage reduced to a value corresponding to a  
14 logical one (i.e., a low impedance will exist between the  
15 source-drain regions of cell 1-1 in response to a voltage  
16 of approximately 5 volts applied to the control gate (word  
17 line 203-1) of cell 1-1). The erase state of each cell  
18 being erased is tested after each erase voltage pulse by  
19 suitable test circuitry preferably contained in the same  
20 integrated circuit device (not shown, but described in the  
21 aforementioned published European patent application).

22 When it has been determined by such test cir-  
23 cuitry that a cell being erased has in fact been erased,  
24 erasure of that cell stops by such test circuitry prevent-  
25 ing additional erase pulses from being applied to its  
26 associated erase line (e.g., erase line 201-1 associated  
27 with cell 1-1).

28  
29 In another embodiment of this invention, a plurality  
30 of cells along a selected word line are erased simulta-  
31 neously, with each cell being erased being self-limited  
32 only by itself. Thus, when a first cell being erased  
33 along a selected word line is sufficiently erased (as  
34 determined after one or more erase pulses by suitable test  
35 circuitry, not shown), its associated erase line is pre-  
36 vented from receiving additional erase pulses, thereby  
37 preventing over-erasure of that cell, while allowing the  
38 remaining cells along the selected word lines which are to

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1 be erased to receive additional erase pulses. The circuit  
2 shown in the schematic diagram of Figure 4 is suitable for  
3 this purpose, merely by adapting Y decoder 205 to provide  
4 the erase voltage pulse VE to a selected plurality of  
5 erase lines 201-1 through 201-M simultaneously.  
6

7 In another embodiment of this invention, a plurality  
8 of cells along a selected bit line are erased simulta-  
9 neously, with each cell being erased being self-limited  
10 only by itself, thus, when a first cell being erased along  
11 a selected bit line is sufficiently erased (as determined  
12 after one or more erase pulses by suitable test circuitry,  
13 not shown), its associated word line is deselected, thereby  
14 preventing the erased cell from being further erased upon  
15 application of additional erase pulses to its erase line,  
16 thereby preventing over-erasure of that cell, while allowing  
17 the remaining cells on the selected bit line to be further  
18 erased upon receipt of additional erase pulses.  
19

20 The present invention alleviates the problem of  
21 insufficient erasure by allowing each cell along either an  
22 individual bit line 202-1 through 202-M or along an indivi-  
23 dual word line 203-1 through 203-N to be independently  
24 erased. However, each cell along a particular bit line  
25 202-1 through 202-M (or word line 203-1 through 203-N can  
26 be erased along with other selected cells along that  
27 particular bit line (or word line), because complete  
28 erasure of one of the cells does not result in a drop in  
29 the voltage along the other bit lines of the cells being  
30 erased.  
31

32 While specific embodiments of this invention have  
33 been presented in the specification, these specific embodi-  
34 ments are intended to serve by way of example only and are  
35 not to be construed as limitations on the scope of this  
36 invention. Numerous other embodiments of this invention  
37 will become readily apparent to those with ordinary skill  
38 in the art in light of the teachings of this specification.

1

CLAIMS

5

1. A memory device comprising a plurality of  $N \times M$  cells (1-1 to N-M), each cell capable of storing a single bit, said device comprising :

10

a plurality of  $N$  word lines (203-1 to 203-N);

a plurality of  $M$  bit lines (202-1 to 202-M);

a plurality of  $M$  erase lines (201-1 to 201-M);

wherein each said cell is associated with one of said plurality of  $N$  word lines, one of said plurality of  $M$  bit lines, and one of said plurality of  $M$  erase lines;

15

characterized in that at least one selected cell is erased by selecting the bit line associated with said at least one selected cell and de-selecting the remaining bit lines, selecting the word line associated with said at least one selected cell and de-selecting the remaining word lines, and applying a plurality of erase pulses to the erase line associated with said at least one selected cell, and in that the contents of each said selected cell is read after each of said plurality of erase pulses, and erasure of said each selected cell is stopped when the contents of said each selected cell has been erased.

25

2. The structure as in Claim 1, characterized in that each said cell comprises :

30

a drain connected to its associated bit line (202);

a source connected to a reference potential;

a floating gate;

a control gate connected to its associated word line (203) and;

35

an erase terminal connected to its associated erase line (201).

1           3. The structure as in Claim 1 or 2, characterized  
in that, during erasure, said word lines (203) are selected  
by the application of a low voltage and deselected by the  
application of a high voltage; and  
5       said bit lines (202) are selected by the application of a  
high voltage, and deselected by the application of a low  
voltage.

          4. The structure as in anyone of claims 1 to 3,  
10       characterized in that said plurality of erase pulses are  
also applied to the bit line associated with said at least  
one selected cell.

          5. The structure as in any one of claims 1 to 4,  
15       characterized in that one selected cell is erased at a time,  
and in that the erasure of said selected cell is stopped by  
terminating the application of said plurality of erase  
pulses when the content of said selected cell has been  
erased.

20           6. The structure as in any one of claims 1 to 4,  
characterized in that a plurality of cells associated with a  
specified word line are erased simultaneously and in that  
the erasure of each selected cell is stopped when said each  
25       selected cell has been erased by preventing said erase  
pulses to be applied to the erase line associated with said  
each erased selected cell,

          whereby the erasure of each erased selected cell  
ceases without ceasing further erasure of the remaining  
30       cells being erased.

1           7. The structure as in any one of claims 1 to 4,  
characterized in that a plurality of cells associated with a  
specified bit line are erased simultaneously, and in that  
the erasure of each selected cell is stopped when said each  
5   selected cell has been erased by deselecting the word line  
associated with said each erased selected cell,

          whereby the erasure of each erased selected cell  
ceases without ceasing further erasure of the remaining  
cells being erased.

10

15

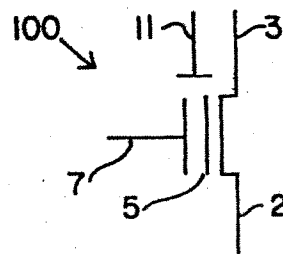
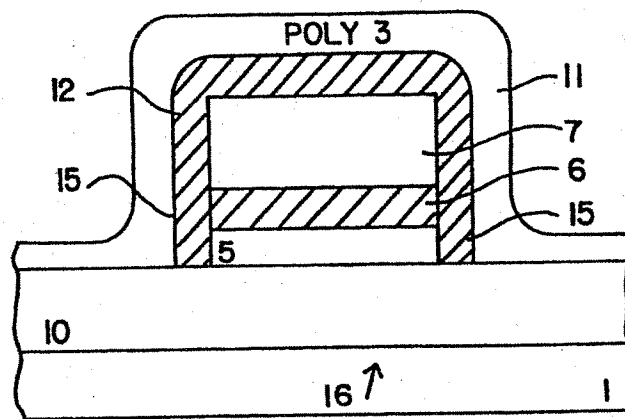
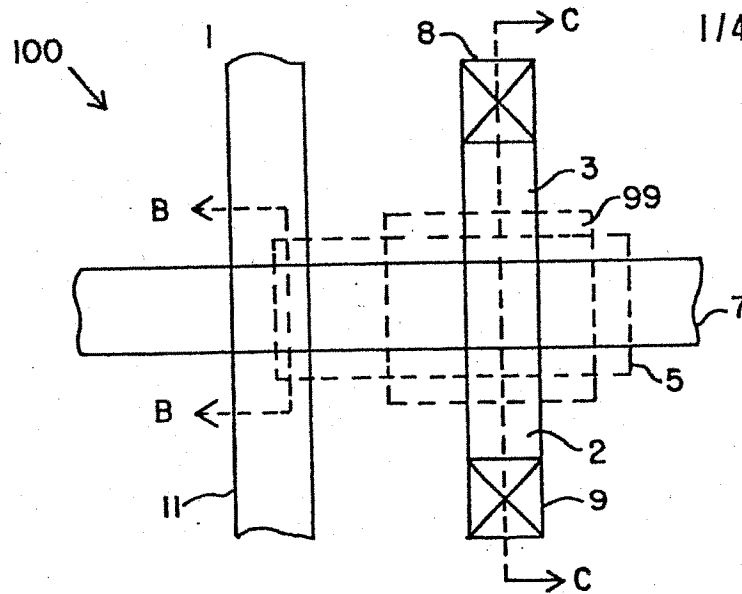
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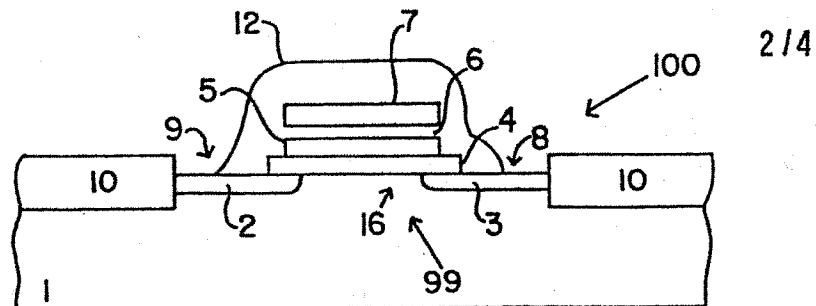


FIG. 1c

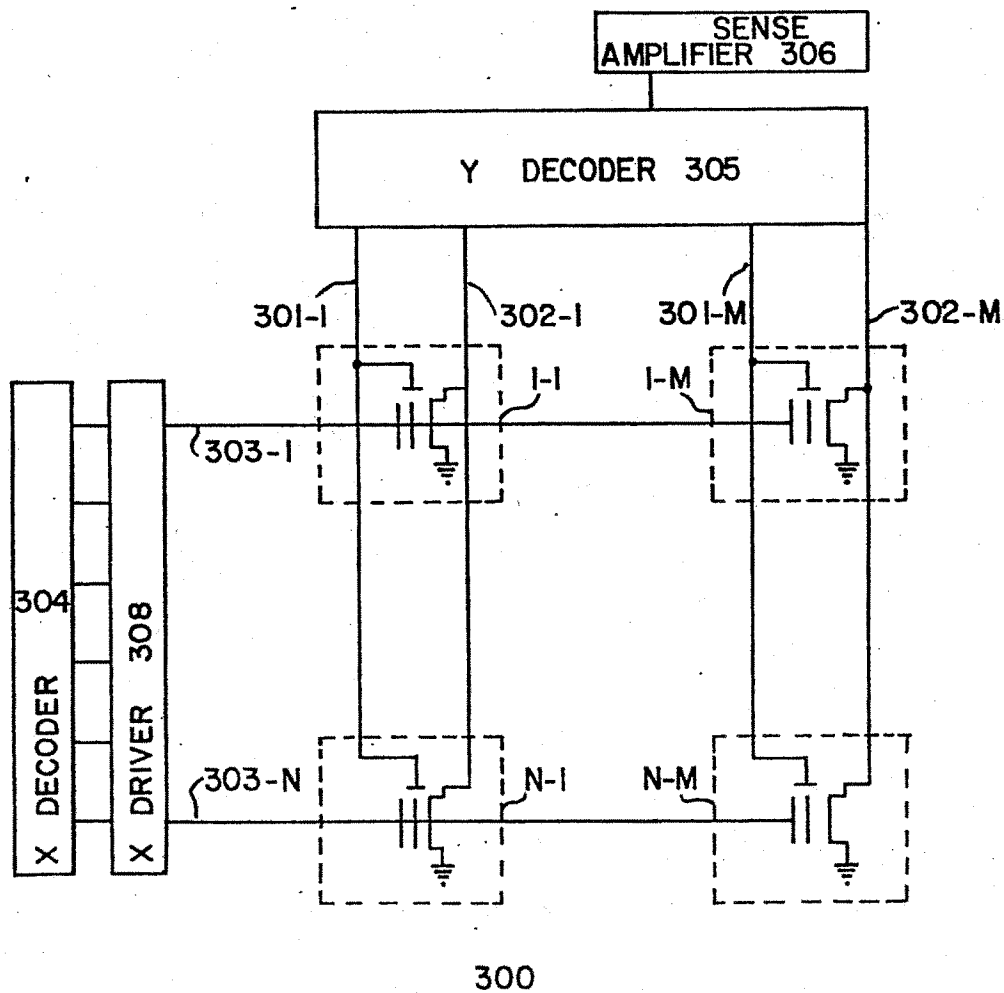
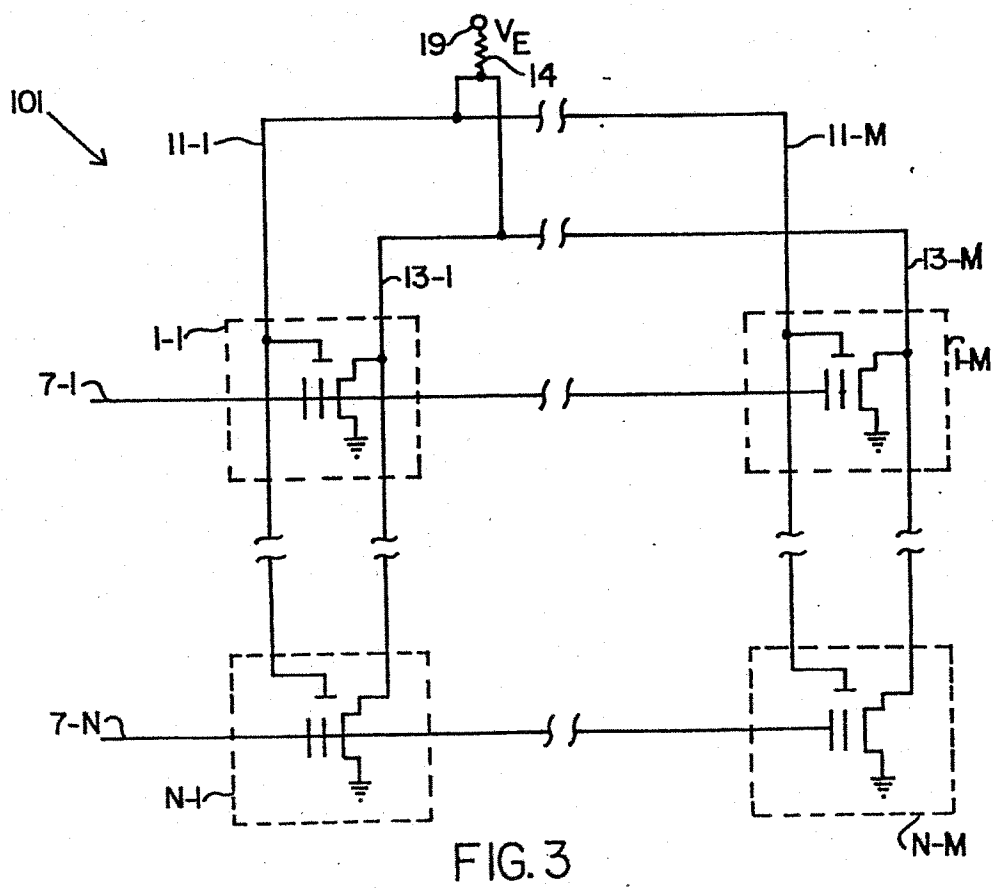


FIG. 2



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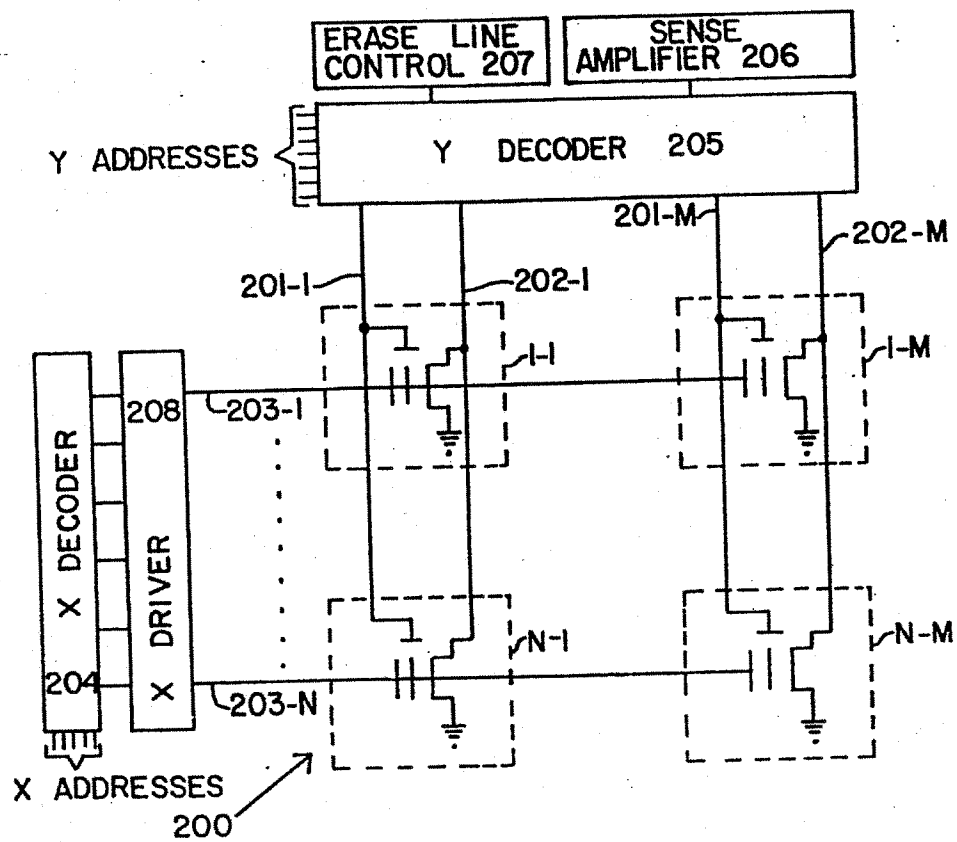


FIG. 4